REMARKS

Claims 1, 8, 11, and 17 have been amended, and claims 2, 10, 12, 13, and 19 have been canceled. Claims 1, 3-9, 11, 14-18, and 20 remain pending in the captioned case. Further examination and reconsideration of the presently claimed application are respectfully requested.

Allowable Subject Matter

Claim 13 was indicated as containing allowable subject matter, and would be allowable is rewritten into independent form including all limitations of the base claim and any intervening claims. In response thereto, the subject matter from claims 10, 12, and 13 has been inserted into independent claim 8. In addition, claim 11 has been amended to reflect dependency to claim 8. Accordingly, Applicants believe claim 8 and claims dependent therefrom are now in condition for allowance.

Section 102 Rejection

Claims 1-5 and 17 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent Publication No. 2003/0107908 to Jang et al. (hereinafter "Jang"). Claims 8, 14, and 16 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,856,937 to Chu et al. (hereinafter "Chu"). Applicants believe in light of the amendment to claim 8, that the rejections of claims 8, 14, and 16 have been obviated in their entirety. Accordingly, the arguments presented below pertain only to the rejection of claim 1-5, and 17.

The standard for "anticipation" is one of fairly strict identity. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art of reference. *Verdegaal Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987); MPEP 2131. Furthermore, anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, as arranged in the claim. *W.L. Gore & Assocs. V. Garlock*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983). Using these standards, Applicants submit the cited art fails to disclose each and every element of the currently pending claims, some distinctive features of which are set forth in more detail below.

Jang does not teach or suggest primary and secondary semiconductor memory devices, each comprising a midpoint between outer lateral edges of each respective primary and secondary semiconductor memory device through which a single axis extends substantially perpendicular to the first and second outside surfaces. Present claim 1 recites the stated limitation. Specifically, claim 1 makes clear that the primary and secondary semiconductor devices arranged on the outer surfaces have outer lateral edges. The outer lateral edges surround a midpoint of those devices. More importantly, the midpoint of the primary memory device and the midpoint of the secondary memory device form an axis, labeled as numeral 22 in Fig. 5 of the present specification. Further details of the single axis 22 which extends substantially perpendicular to the first and second outside surfaces are set forth in the originally-filed specification, for example, page 11, lines 10-22. Since the single axis 22 is perpendicular to the first and second outside surface, the lateral edges around each midpoint of both the primary and secondary memory devices must be aligned directly opposite one another, with no offset whatsoever.

Contrary to present claim 1, Jang makes no mention whatsoever of a midpoint for the semiconductor devices 150 and 150' (Jang -- Figs. 5A-5C). In fact, there is no midpoint shown or described anywhere in Jang. The midpoint referred to in the Office Action is the midpoint of via 531, not the midpoint between lateral edges of the integrated circuits 150 and 150'. Absent any disclosure of a midpoint of the integrated circuit, Jang also lacks any teaching of the midpoints forming a single axis perpendicular to the opposed outer surfaces of board 510. Instead, integrated circuit 150 may be larger than integrated circuit 150', even though one lateral edge may be directly opposite the other. The larger integrated circuit would have a midpoint skewed or offset from the smaller integrated circuit, even though one lateral edge is aligned as shown in Fig. 5 of Jang. Any such skewing or offset between midpoints would cause the axis to no longer exist perpendicular to the opposed surfaces. Accordingly, the rejection of claim 1 and claims dependent therefrom is respectfully traversed.

Jang does not teach or suggest terminating the opposing first and second ends of the conductor with a pull-up resistor to a power supply having a voltage value dissimilar from a voltage value placed on the pair of packaged memory devices. Present claim 17 describes a power supply having a voltage value applied to a pull-up resistor that is different from a voltage value placed on the pair of packaged memory devices. The limitation of claim 19 which has been placed into independent claim 17 is similar to the limitation of claim 13 which was

deemed to contain allowable subject matter. Specifically, the Office Action notes that the prior art does not teach or suggest a reference supply applied to a pull-up resistor through a first power supply conductor and another power supply coupled to the primary and secondary SDRAMs through the other power supply conductor. Claims 8 and 17 both now recite two different power supplies (a power supply used by the SDRAM and a power supply or reference supply applied to the pull-up resistors). Accordingly, Applicants believe claim 17 and claims dependent therefrom are now patentable over the cited art.

For at least the reasons set forth above, Applicants assert that independent claims 1 and 17 and claims dependent therefrom, are not anticipated by the cited art. Therefore, Applicants respectfully request removal of this rejection.

Section 103 Rejection

Claim 6, 7, and 18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Jang in view of Chu. Claim 9 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Chu in view of Jang. Claims 10-12 and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chu in view of U.S. Patent No. 5,945,886 to Millar (hereinafter "Millar"). Claim 19 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Jang in view of U.S. Publication No. 2003/0137860 to Khatri et al. (hereinafter "Khatri"). Claim 20 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Jang in view of Millar.

Claims 10 and 12 have been canceled rendering rejection thereto moot. In addition, Applicants believe in light of the amendments to claim 8 and 17, that the rejections of claims 9, 11, 15, and 18-20 have been obviated in their entirety. In addition, Applicants believe dependent claims 6 and 7 are patentable over the cited art for the same reasons as their base claim 1. Therefore, Applicants respectfully request removal of this rejection.

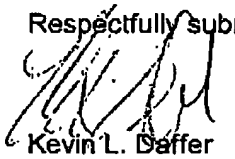
CONCLUSION

The present amendment and response is believed to be a complete response to the issues raised in the Office Action mailed June 14, 2005. In view of the remarks traversing the rejections, Applicant asserts that pending claims 1, 3-9, 11, 14-18, and 20 are in condition for

allowance. If the Examiner has any questions, comments or suggestions, the undersigned attorney earnestly requests a telephone conference.

No fees are required for filing this amendment; however, the Commissioner is authorized to charge any additional fees that may be required, or credit any overpayment, to LSI Logic Corp. Deposit Account No. 12-2252/03-1236.

Respectfully submitted,



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Date: September 14, 2005